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METHODS OF DESIGNING ANALOG-TO-DIGITAL CONVERTERS

Master's Thesis Presentation

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Purpose

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The purpose is to investigate the design of 14-bit resolution ADC with sampling frequency 2 MHz in 0.13 um technology.

ADC architectures

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Comparison table

Architecture	Speed	Conversion time	Resolution	Area	Power consumption
Flash ADC	High	Constant	Low (up till 8 bits)	Increases exponentially with resolution	Very high
Pipelined ADC	Medium -high	Increases with resolution	Medium-high (up till 12-bits)	Increases linearly with resolution	Medium
Sigma-Delta ADC	Medium	Trade off with resolution	High (up till 24-bits)	Constant; no change with increase in resolution	Medium-low
SAR ADC	Medium -low	Increases with resolution	High (up till 18-bits)	Increases linearly with resolution	Medium-low

Spec

Resolution

- **14 bit**

Frequency

- **2 MHz**

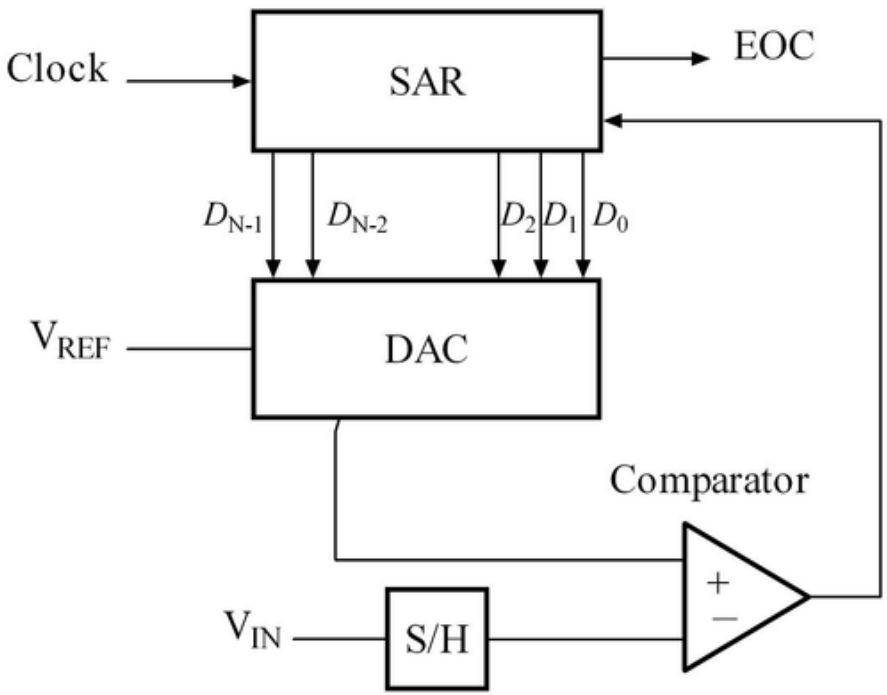
Technology

- **SG13S**

Power supply

- **1.2 V**

Successive approximation ADC



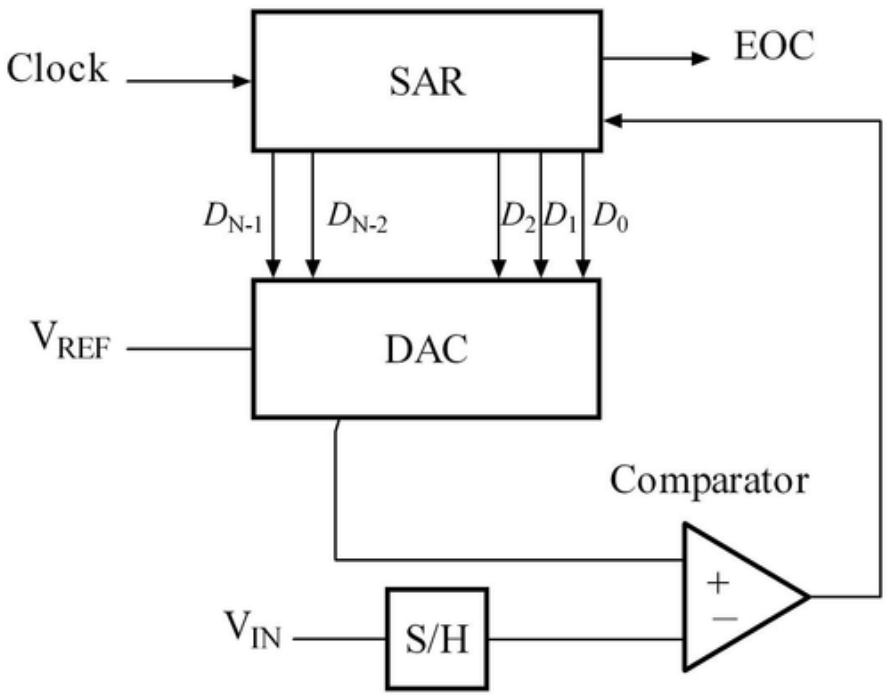
Advantages

- Low power consumption,
- Low circuit complexity
- Mostly digital circuitry.

Limitations

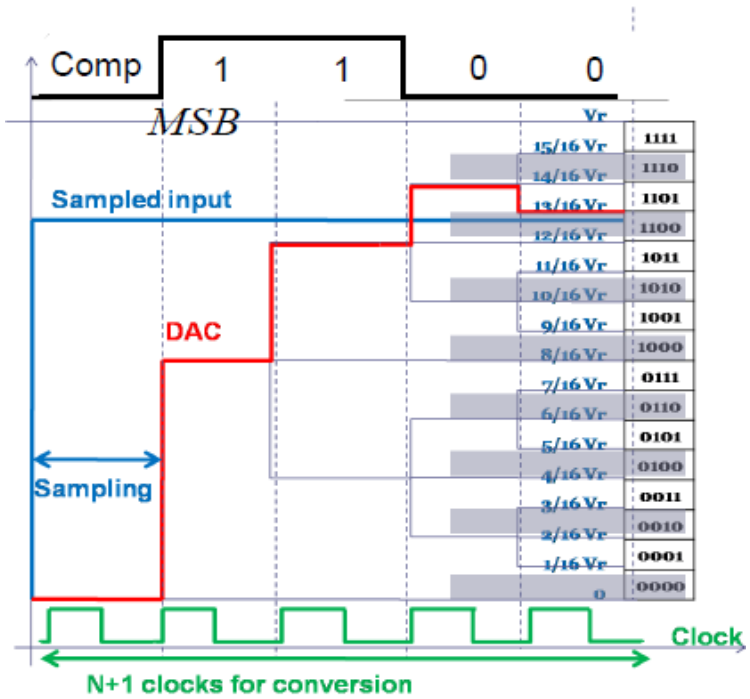
- Lower sampling rates
- Accuracy of the system depends of the accuracy of the DAC and the comparator.

Successive approximation ADC

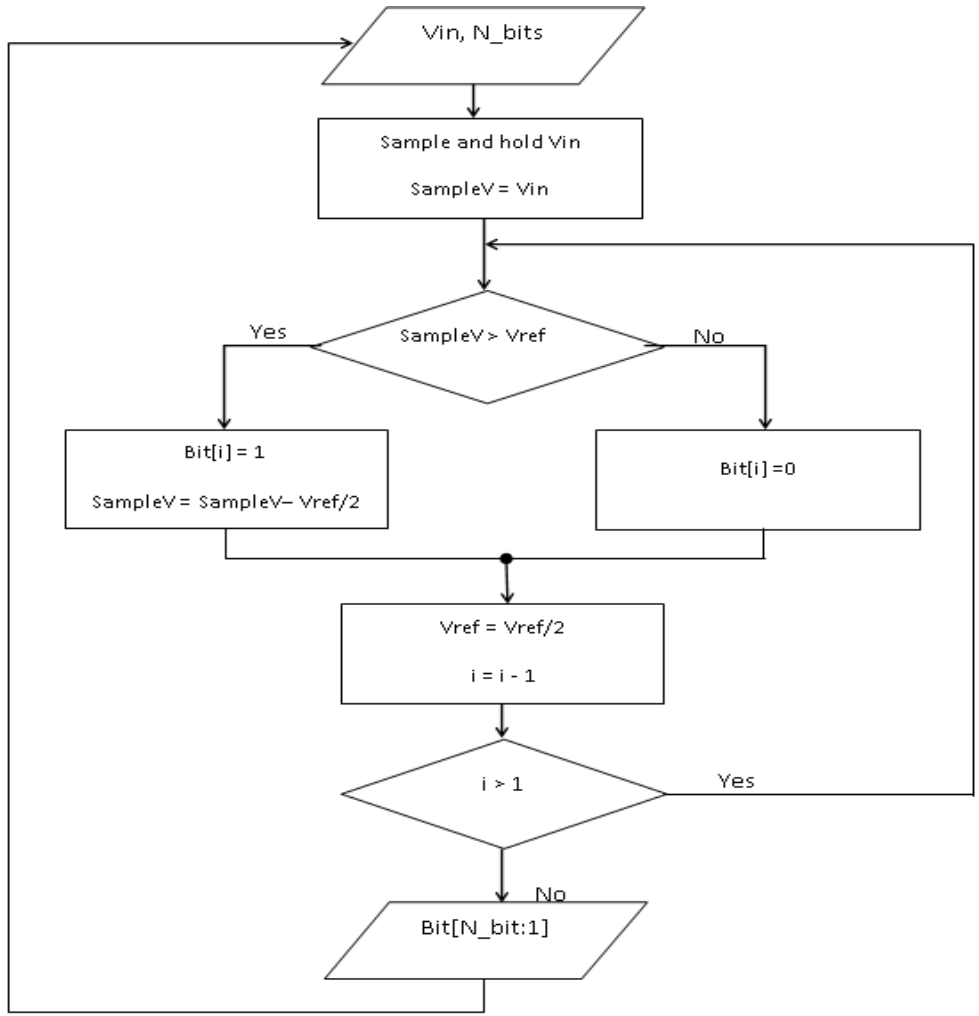


$$Vin = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$

Principle of operation



Mathematical model



Mathematical model

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Imperfections

Offset voltage

Jitter

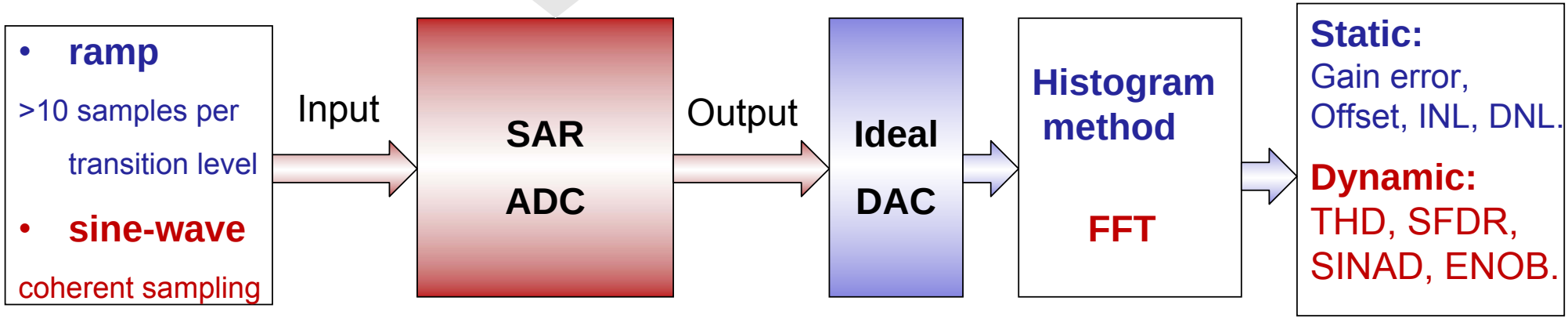
Thermal noise

Settling time limitations

Clock feedthrough

Mismatches

Parasitic capacitance



Modeling of Capacitor array mismatch effect

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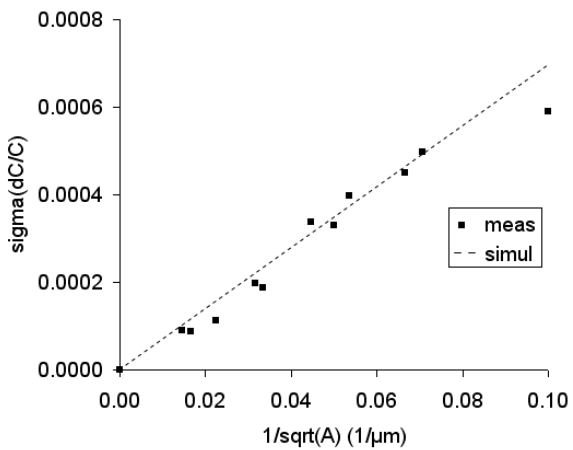
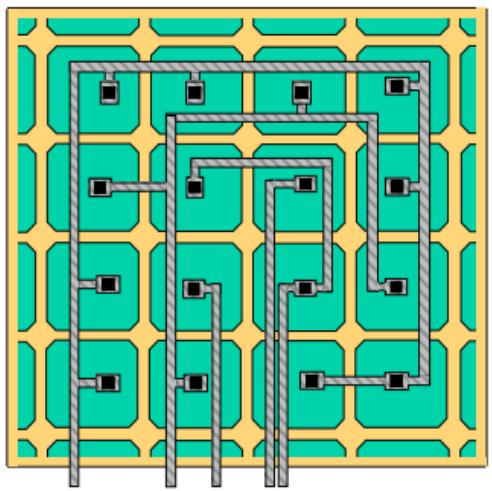
Pelgrom's Law :

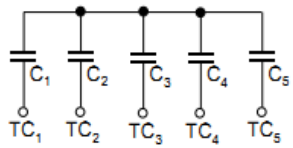
$$\delta\left(\frac{\Delta C}{C}\right) = \frac{K_p}{\sqrt{WL}}$$

K_p- is matching parameter



Common centroid structure





$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

$$C_i = 2^{i-1}C_1, \quad i = 1, N$$

$$\delta_{C_i} = \frac{\delta_{C_1}}{\sqrt{2^{i-1}}}$$

Elena Shvaichenko

Simulation results of modeling Capacitor array mismatch effect

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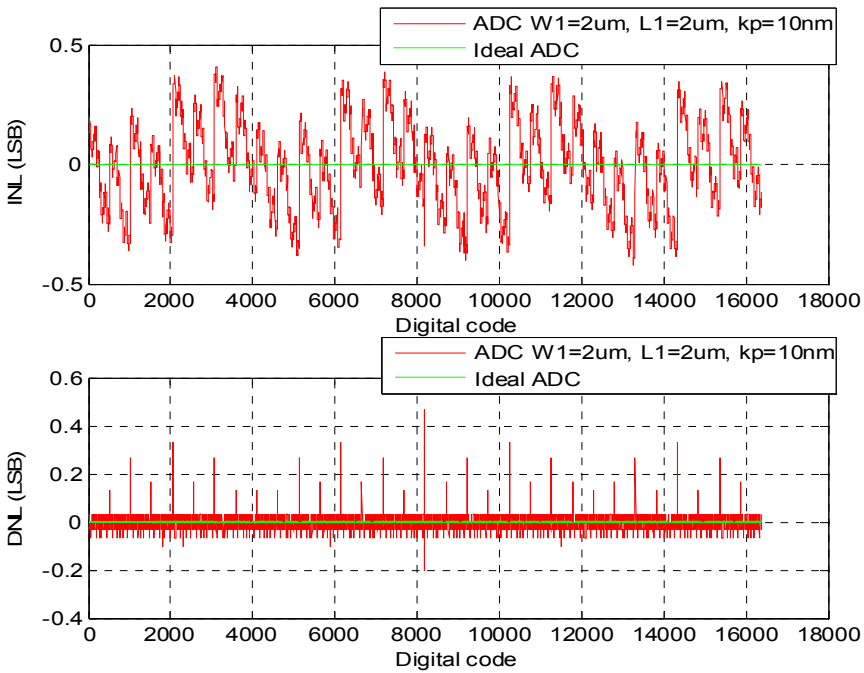

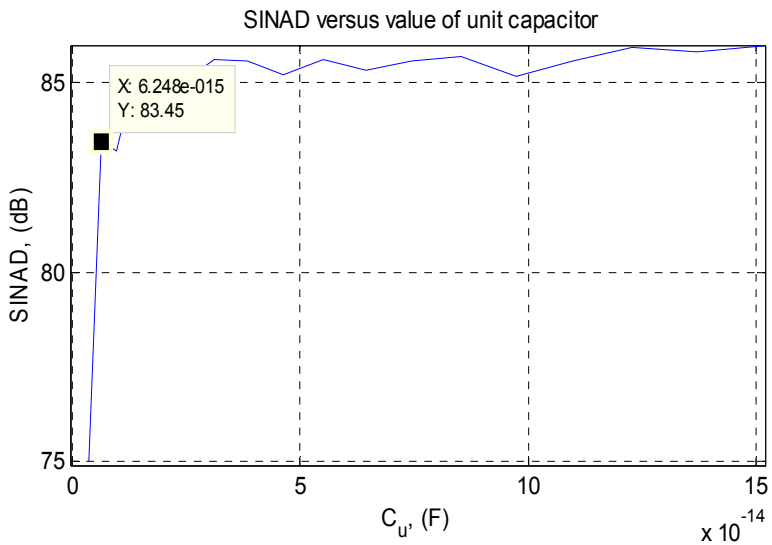

Mismatch → Cu = 6.5 fF

Modeling of Settling time effect

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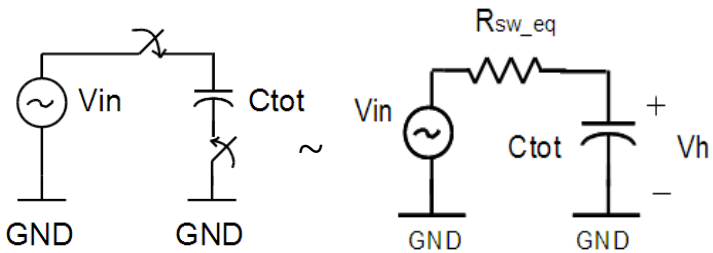
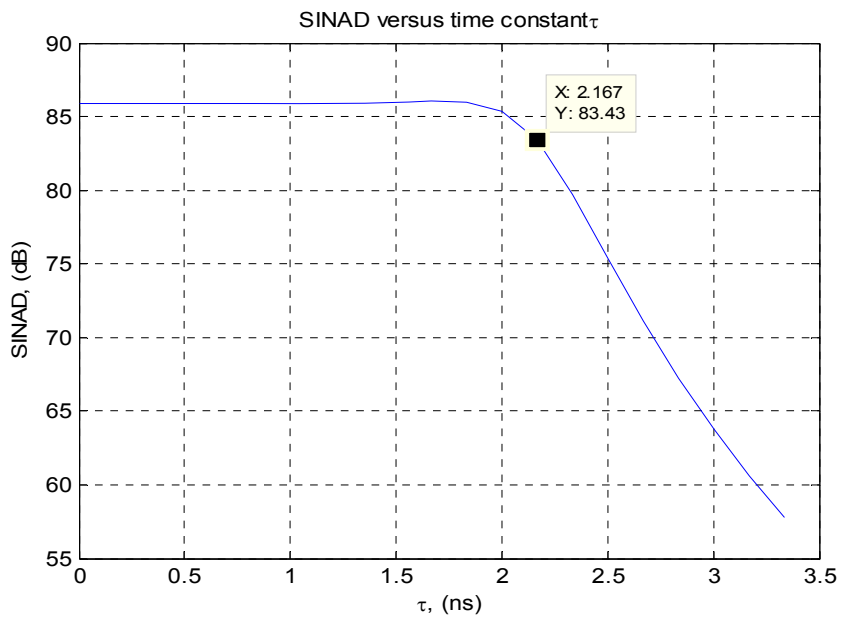
Sampling phase



$$V_h = V_{in}\left(1 - e^{-\frac{tclk}{\tau}}\right)$$

$$t_{clk} = \frac{1}{N_{cycles} f_s} >> \tau = R_{sw\_eq} C_{tot}$$

$$R_{sw} = \frac{1}{C_{ox}\mu_{eff} W/L (V_{GS} - V_t)}$$



Sampling frequency → Switches sizing.

Behavioural model

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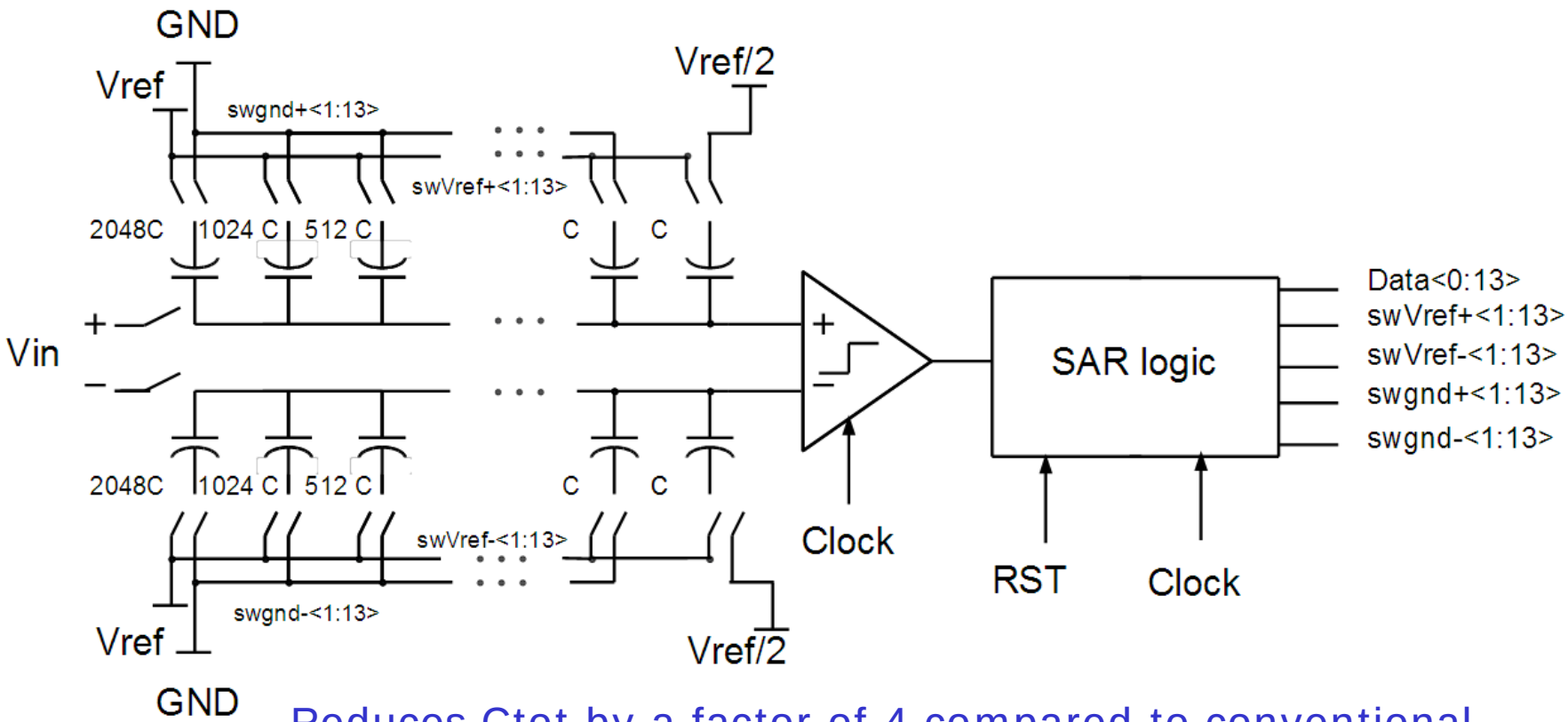
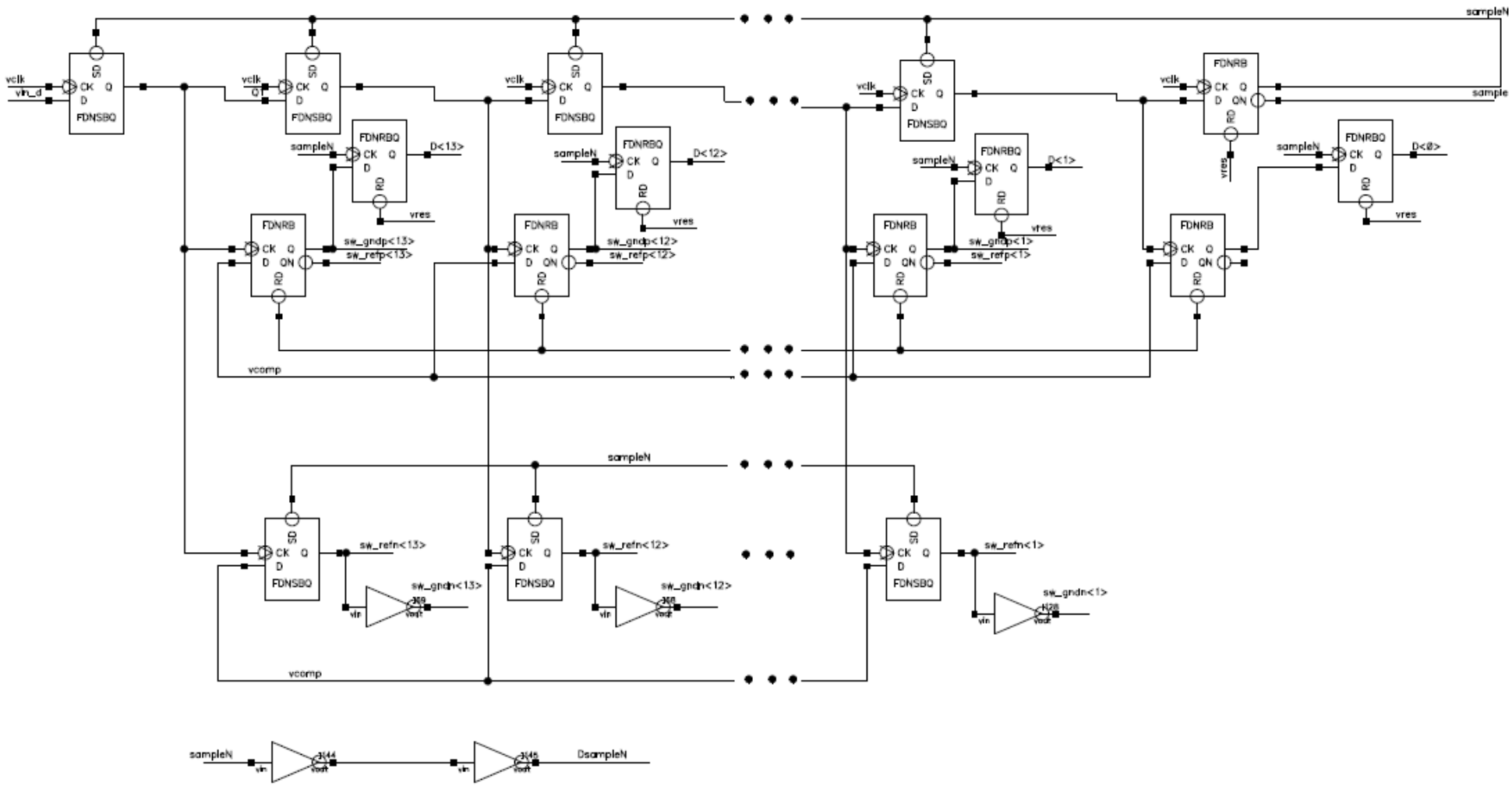
Differential triple reference charge-redistribution SAR ADC with monotonic switching procedure

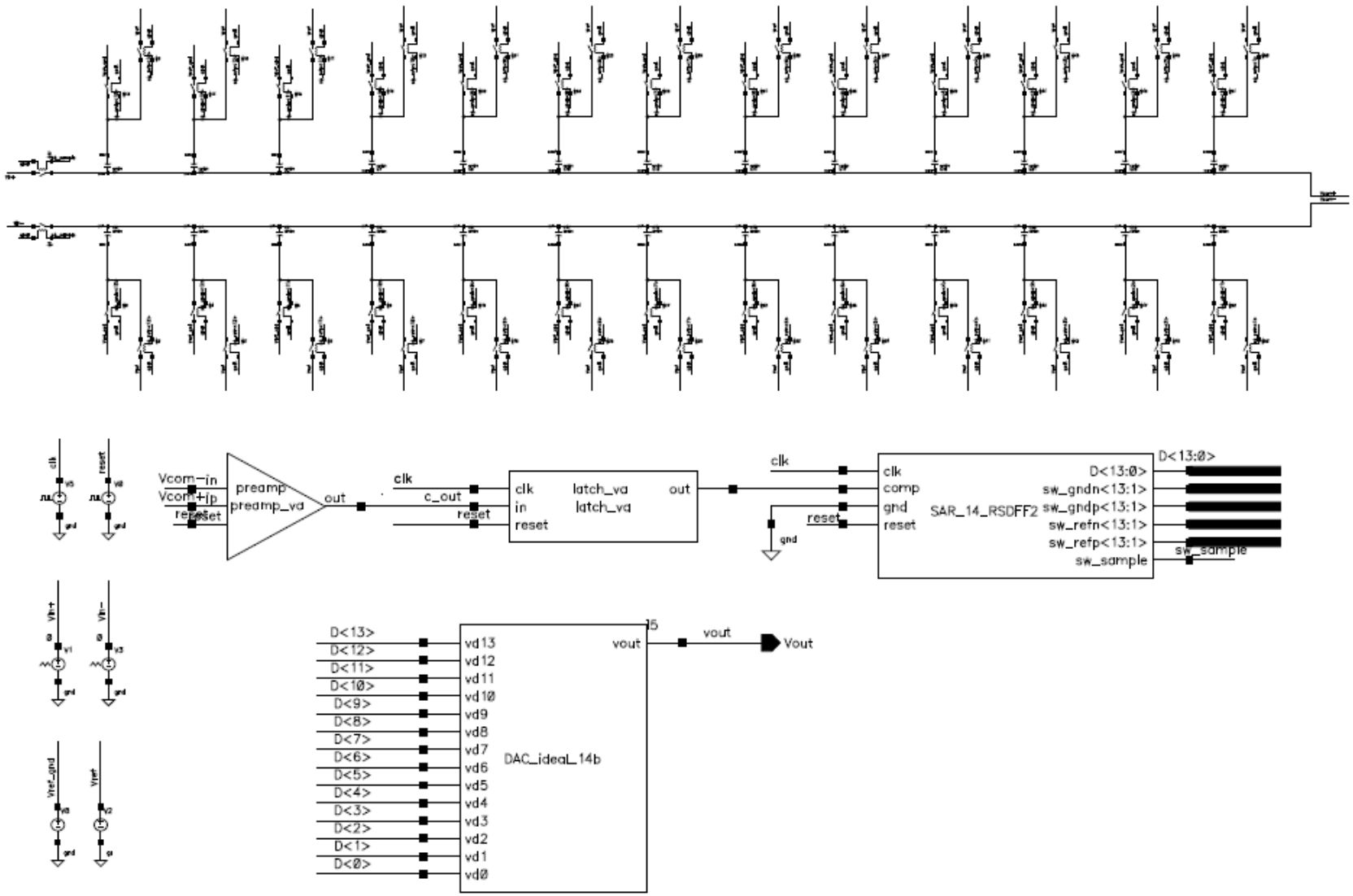


Reduces Ctot by a factor of 4 compared to conventional

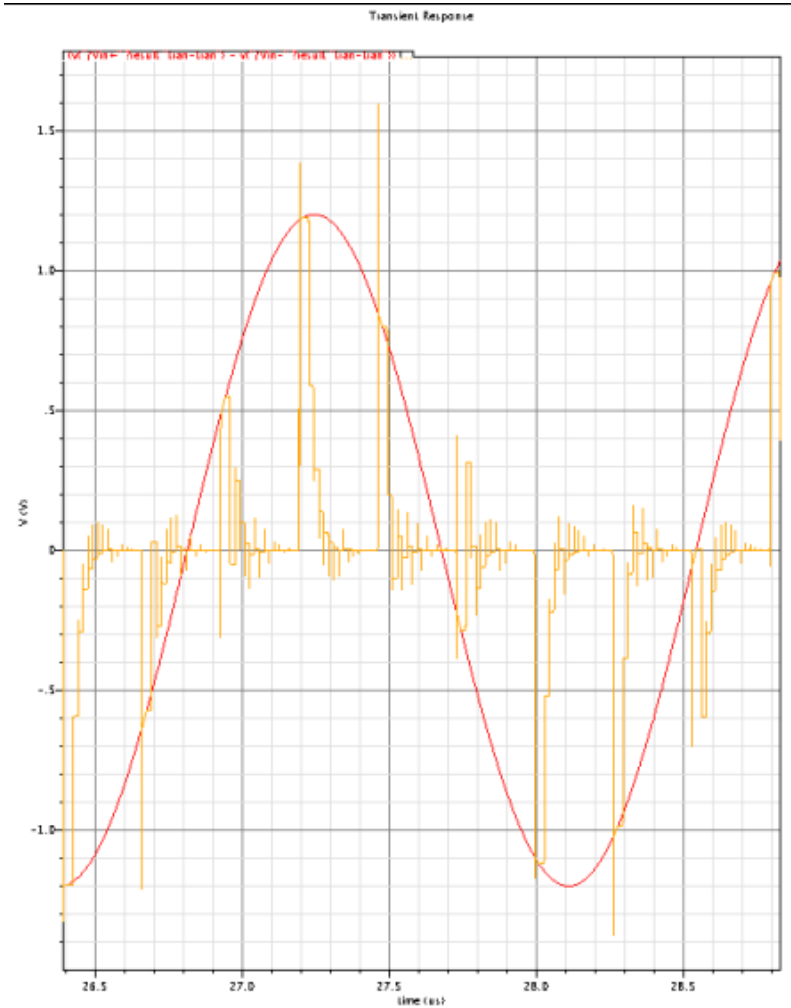
SAR Logic

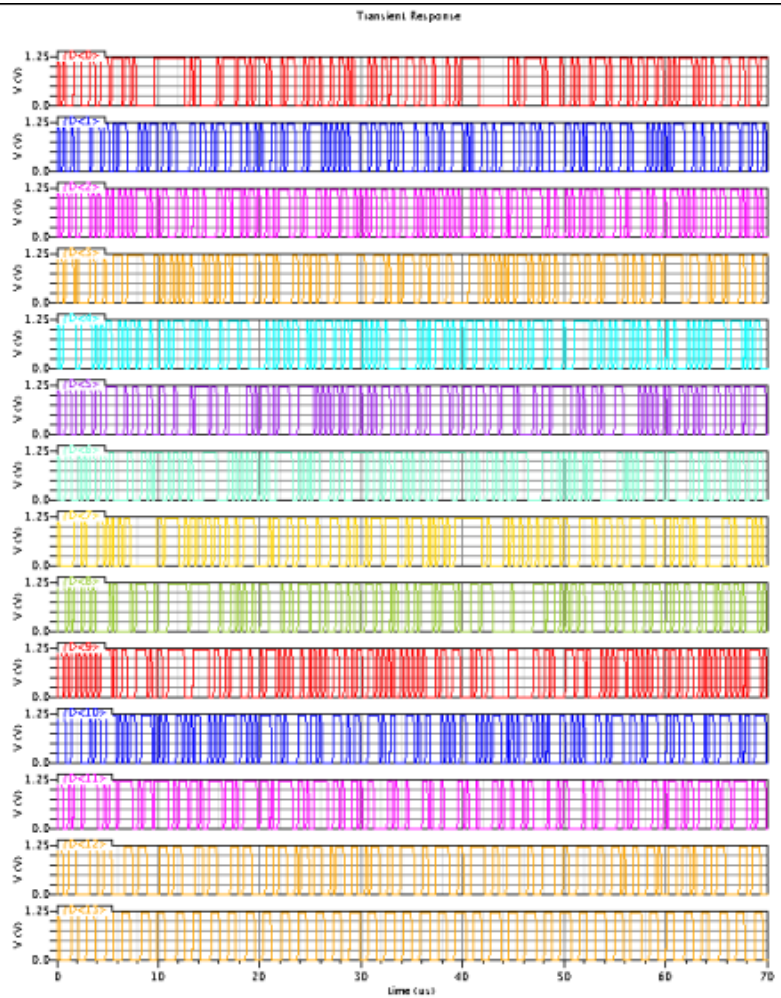


Behavioural model test bench



Simulation results of behavioral model





Simulation results of behavioral model

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Transistor level model

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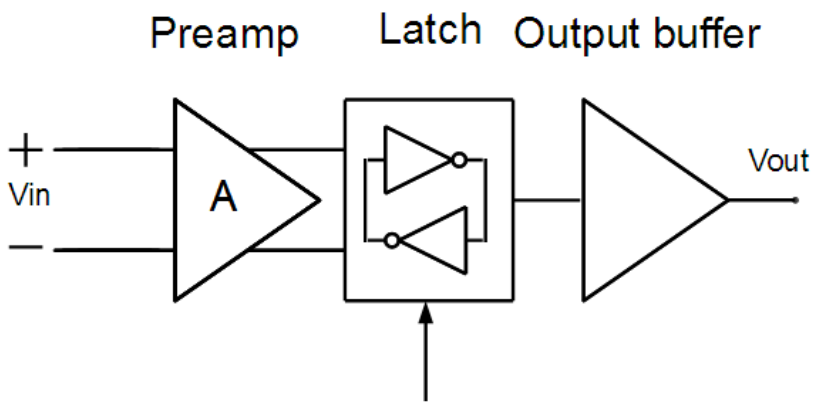
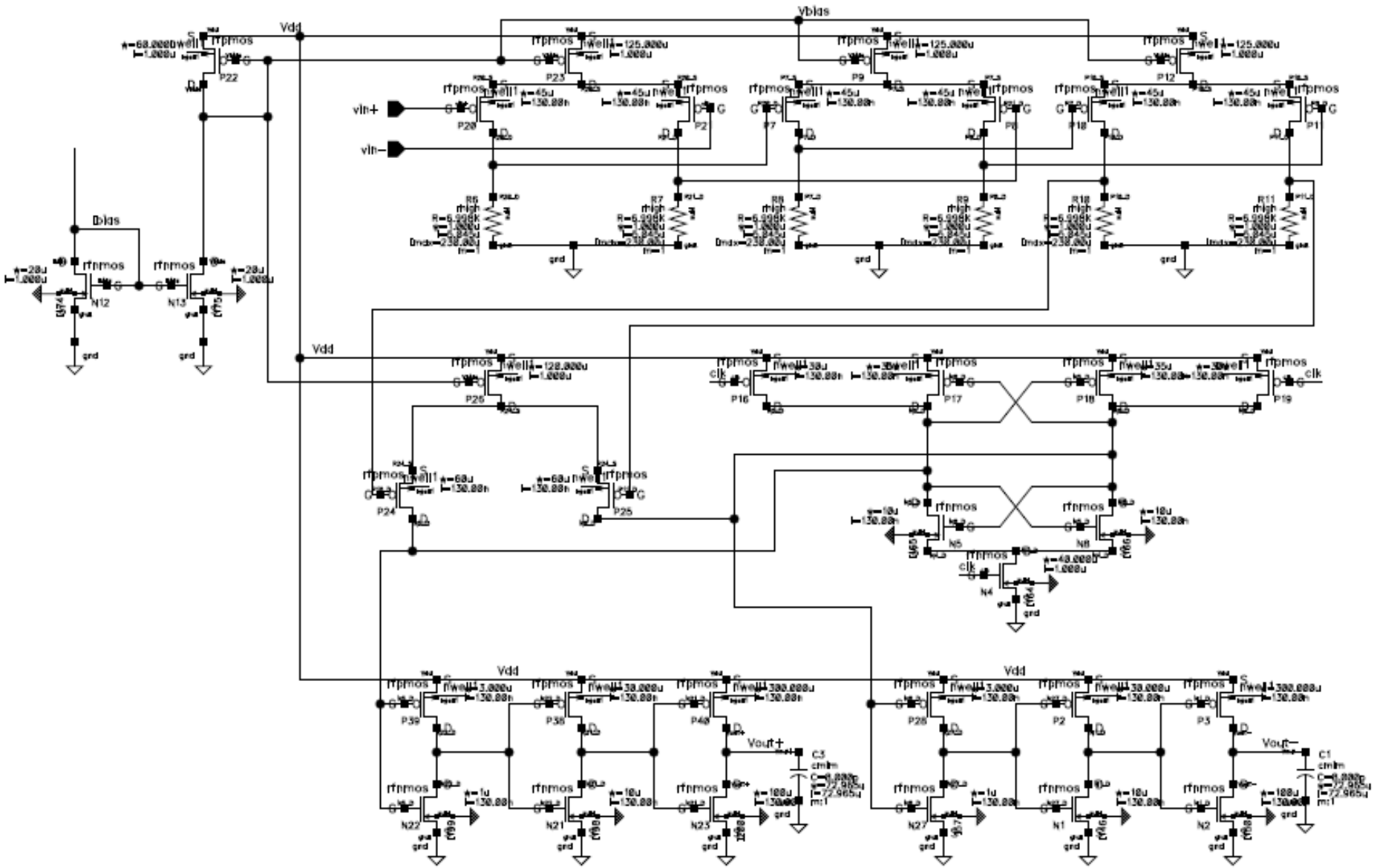
Comparator architecture



Comparator schematic



Simulation results

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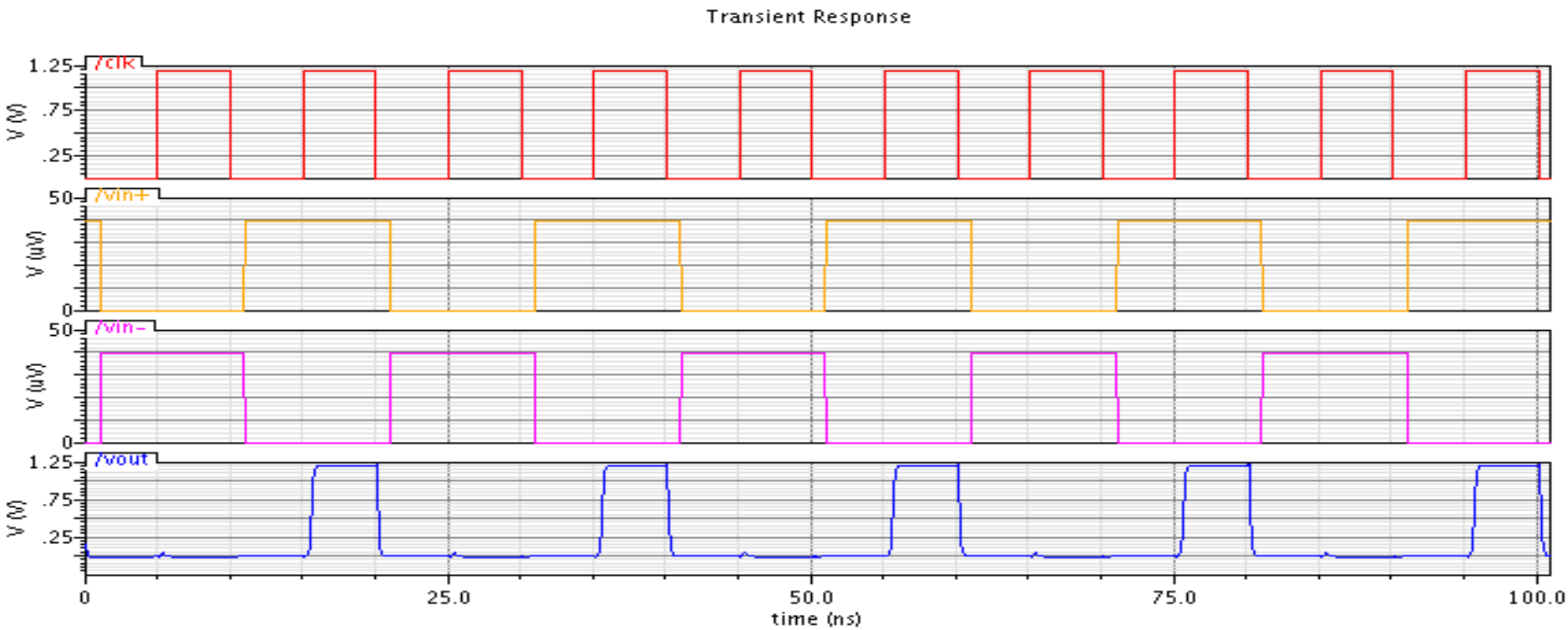
Input and output waveforms



Conclusion

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- ✓ Analysis of ADC architectures was done.
- ✓ SAR architecture was chosen as most appropriate architecture to meet given specification.
- ✓ Development of program for modeling successive-approximation analog-to-digital conversion in MATLAB was done.
- ✓ Analysis of non–ideal effects in SAR ADC was done.
- ✓ Modeling of mismatch, input referred dc offset and settling time effects was done.
- ✓ Simulation of modeling mismatch effect shows that for SG013S IHP technology it is possible to get DNL ≤ 0.5 LSB, INL < 0.5 LSB, THD = -95.07 dB, SFDR = 85.75 dB, SINAD =84.84 dB, ENOB = 13.8 bit with probability 99.7%.
- ✓ Simulation of modeling comparator offset voltage effect shows that for SG013S IHP technology with 3.2 mV input referred dc offset it is possible to get THD = -84.33 dB, SFDR = 76.10 dB, SINAD =74.95 dB, ENOB = 12.16 bit with probability 99.7%.

Conclusion

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✓ Simulation of modeling settling time effect shows that for SG013S IHP technology with 2.1 ns time constant it is possible to get SFDR = 83.97 dB, SINAD =83.7 dB, ENOB = 13.61 bit with probability 99.7%.

✓ Verilog–A behavioral model of 14-bit differential charge–redistribution SAR ADC with monotonic switching procedure was developed.

✓ Simulation of proposed high-speed comparator with resolution 40uV, clock frequency 100 MHz, supply voltage 1.2 V in SG013S IHP technology was done.

✓ Analysis of more than 45 scientific sources up to 2011 year in the field of analog-to-digital conversion has been conducted.

Results of investigation have been published at the International conference on system analysis and information technologies.

The investigation was carried out for IHP - Innovations for High Performance Microelectronics company.

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Thank You!!!

General concept in designing ADC

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Design flow for ADC

- **Mathematical model**
  - Algorithm is examined
  - Functional description

  Abstract model in Matlab, C/C++
- **Behavioural model**
  - Architecture is verified
  - Behavioural description

  of the blocks

  Verilog/VHDL model of the digital part;

  Verilog-A/VHDL- AMS model for the analog

  Synthesis to get gate level Verilog or VHDL
- **Transistor level model**
  - Schematic is verified
  - Transistor level of the blocks

  Schematic design of the analog

  Mixed verification
- **Layout level**

  Analog layout

  Place&Rout of the digital

  Post-layout simulation

Modeling of Capacitor array mismatch effect

If standard deviation of unit capacitance is defined as

$$s_{C_1} = s\left(\frac{\Delta C_1}{C_1}\right) = \frac{K_p}{\sqrt{W_1 L_1}}$$

$$s(\Delta C_1) = C_1 s_{C_1}$$

The next capacitor will be parallel connection of 2 unit capacitor and it's mismatch will be the sum of unit capacitor mismatches. Since this mismatches are independent random variables with Gaussian distributions, the standard deviations
can be related as follows.

$$s(\Delta C_2) = \sqrt{\left(C_1 s_{C_1}\right)^2 + \left(C_1 s_{C_1}\right)^2} = C_1 s_{C_1}\sqrt{2}$$

$$s_{C_2} = s\left(\frac{\Delta C_2}{C_2}\right) = \frac{C_1 s_{C_1}\sqrt{2}}{C_2} = \frac{C_1 s_{C_1}\sqrt{2}}{2C_1} = \frac{s_{C_1}}{\sqrt{2}}$$

Thus for

$$C_i = 2^{i-1} C_1$$

$$s_{C_i} = \frac{s_{C_1}}{\sqrt{2^{i-1}}}$$

Simulation results of modeling Settling time effect

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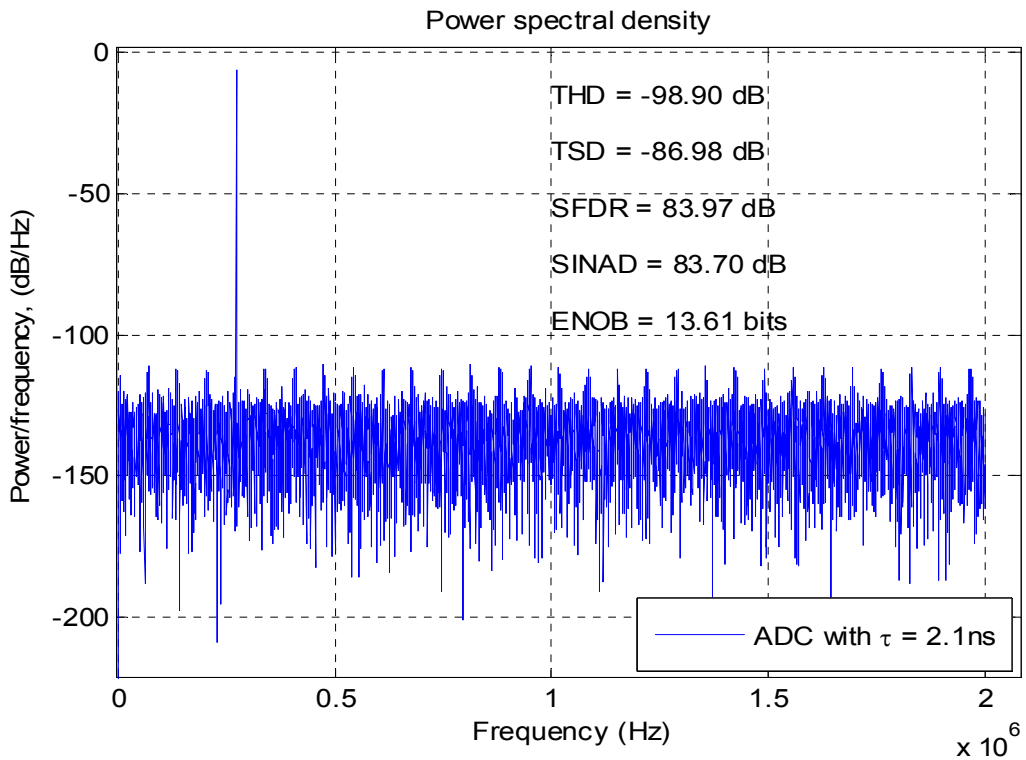
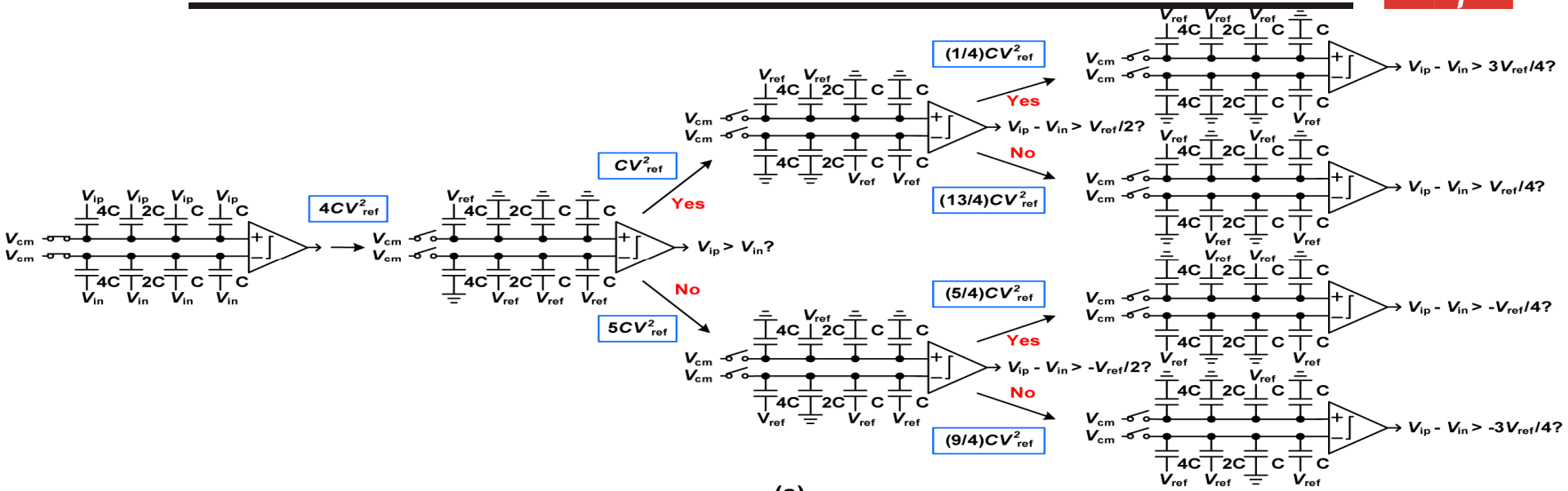
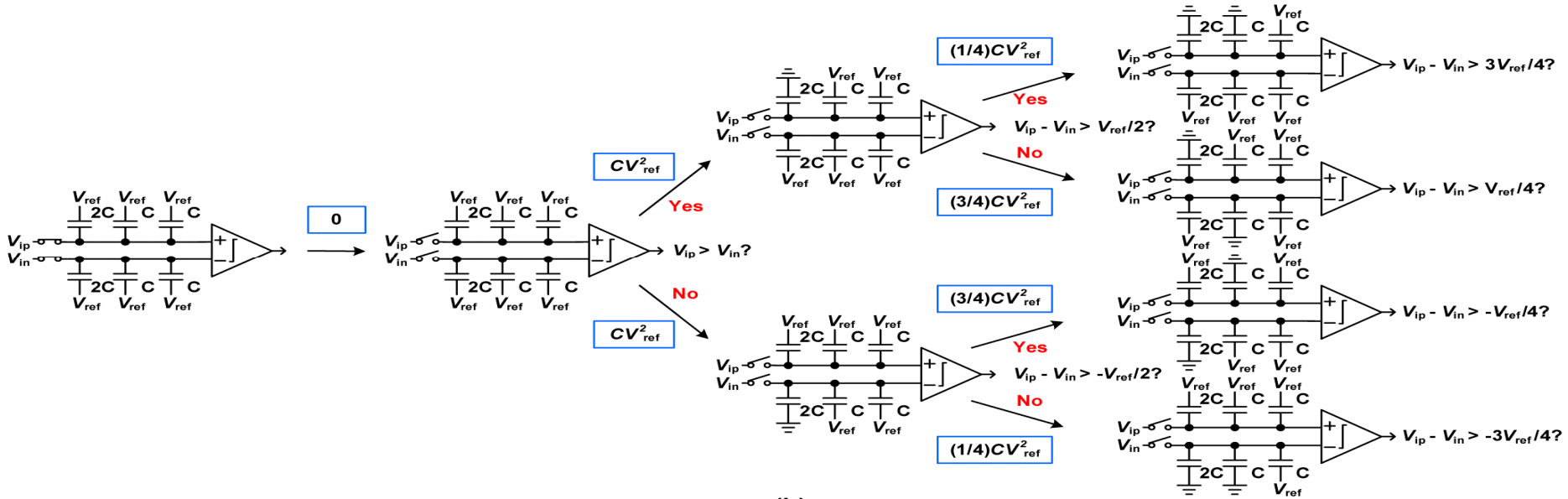


Waveforms of conventional and monotonic switching procedure



(a)



(b)

Waveforms of conventional and monotonic switching procedure

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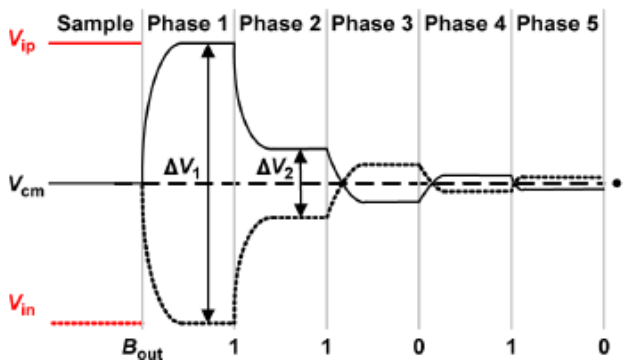
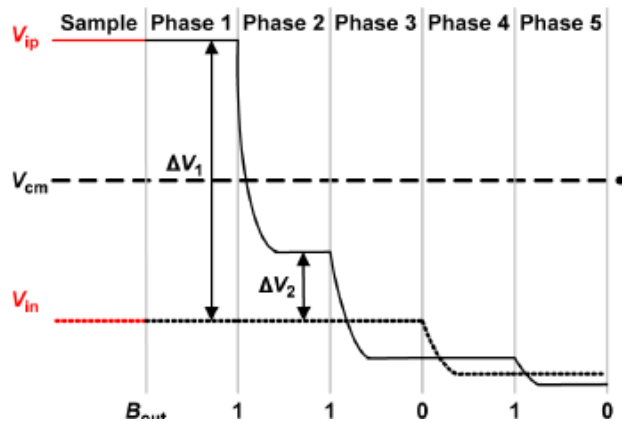
Waveform of conventional switching procedure



Waveform of monotonic switching procedure



Reduces Switching power in a factor of 5

Preamplifiers

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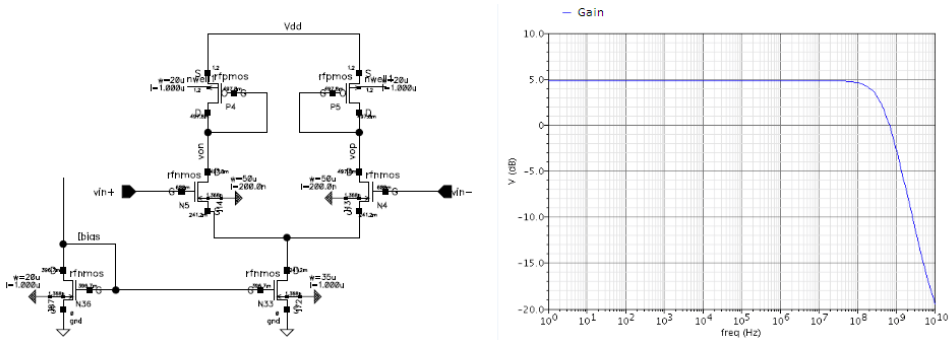
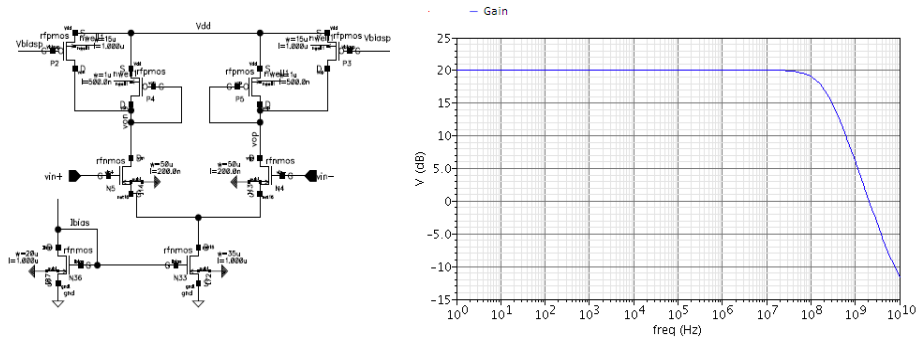
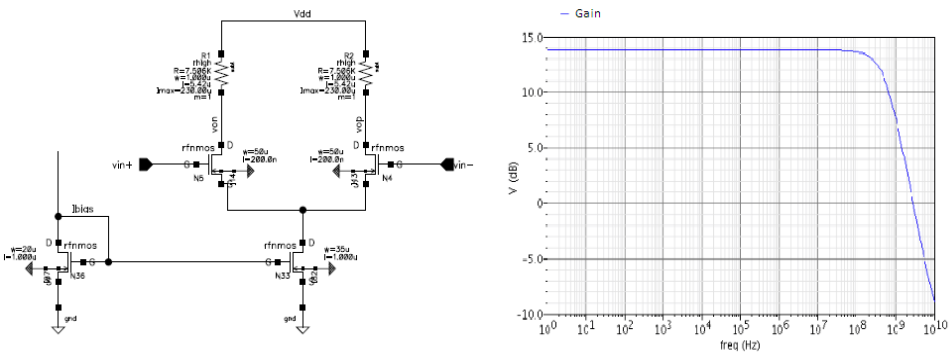


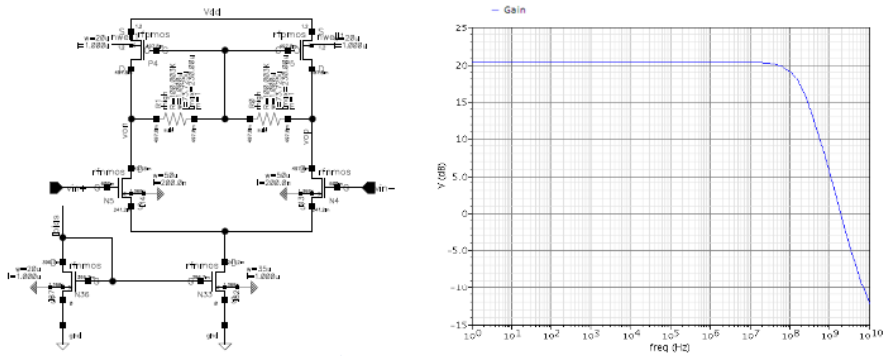
Preamplifier with diode connected pMOS load and it's gain



Modified Bult's preamplifier and it's gain



Preamplifier with resistor load and it's gain



Song's preamplifier and it's gain

Transistor level model

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Preamplifier

Amplifier architecture	Gain, dB	Bandwidth, Hz
Differential pair with resistive load	13.88	565.7
Differential pair with pmos diode connected load	4.86	465.2
Modified Built's preamplifier	20.13	201.3
Song's preamplifier	20.42	178.1

Transistor level model

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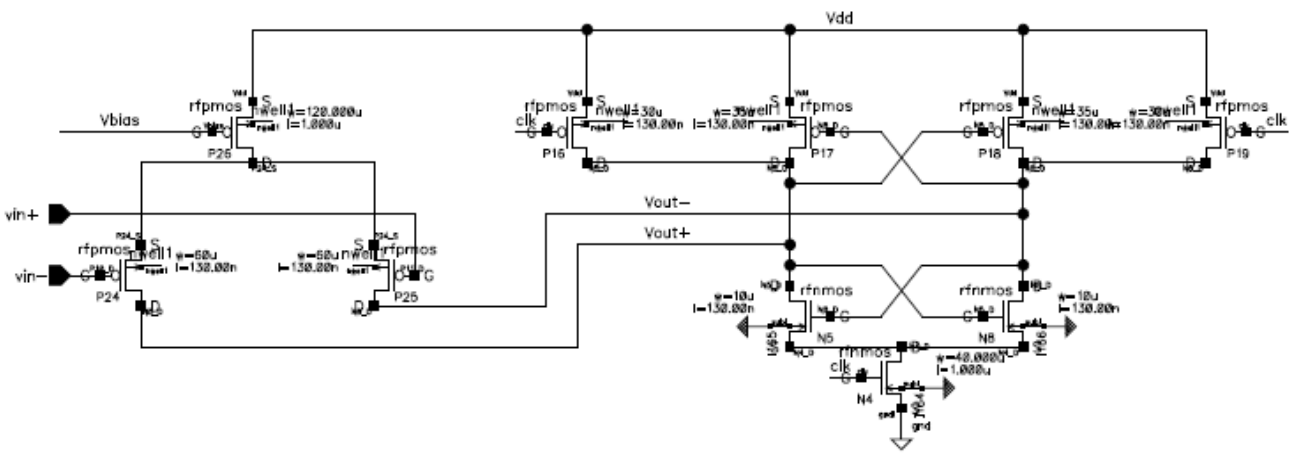
Latch

Dynamic latch



Advantages

ero dc current in reset mode,

ull logic levels after

generation,

outputs are both reset to supply

oltage so they are well defined